AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A process for removing contaminants from a surface of a first material layer during fabrication of an integrated circuit prior to depositing a second material layer thereover, the process comprising steps of:

(a) cleaning the surface;

(b) forming a hydrogen termination on the surface;

(b2) pre-heating the surface, wherein contaminants are formed on the surface;

(c) exposing the surface to a nitrogen-containing gas at a temperature of between about 500°C and 800°C to remove the contaminants from the surface;

(d) depositing the second material layer within the temperature range of the step (c); and

(e) wherein the steps (c) and (d) are performed in a single deposition chamber.

2. (Original) The process of claim 1 wherein the surface comprises a surface of a material layer selected from among a doped epitaxial material, an un-doped epitaxial material, a doped bulk silicon substrate and an un-doped bulk silicon substrate.

3. (Previously presented) The process of claim 1 wherein the a step (a) further comprises:

(a1) subjecting the surface to an HF dip; and

(a2) cleaning the surface using an RCA cleaning process;

4. (Previously presented) The process of claim 1 wherein the step (b) further comprises:

(b1) subjecting the surface to an HF dip; and

(b2) drying the surface with isopropyl alcohol.

5. (Original) The process of claim 1 wherein the nitrogen-containing gas comprises nitrogen fluoride.

6. (Canceled)

7. (Previously presented) The process of claim 1 wherein a duration of the step (c) is between about 20 seconds and 80 seconds.

8. (Canceled)

9. (Previously presented) The process of claim 1 wherein the step (c) is practiced at about 700°C for a duration of about 20 seconds at a flow rate of about 75 sccm.

10. (Previously presented) The process of claim 1 wherein the second material layer is selected from between a doped polysilicon material and an un-doped polysilicon material.

11. (Previously presented) The process of claim 1 wherein the steps (a), (b), (c) and (d) are performed in a single chamber.

12. (Previously presented) The process of claim 1 wherein during execution of the steps (a), (b), (c) and (d) a pressure is maintained at a relatively constant value.

13. (Canceled)

14. (Previously presented) The process of claim 1 wherein the step (c) further comprises subjecting the surface to a hydrogen bake.

15. (Previously presented) The process of claim 14 wherein the step (c) further comprises supplying hydrogen for a duration of about 60 to 90 seconds at a temperature of about 700°C.

16. (Previously presented) The process of claim 14 wherein the second material layer is selected from between a doped polysilicon material and an un-doped polysilicon material.

17. (Previously presented) The process of claim 14 wherein the steps (a) through (d) are performed in-situ.

18. (Previously presented) The process of claim 1 wherein the second material layer comprises an arsenic-doped polysilicon material.

19. (Currently Amended) A process for removing contaminants from a surface of a semiconductor device during fabrication of an integrated circuit, comprising steps of:

(a) exposing the surface to a nitrogen-containing gas at a temperature range of between about 500°C and 800°C and at a flow rate to remove contaminants from the surface; ~~and~~

(b) depositing a polysilicon layer on the surface in situ within the temperature range; and

(b2) pre-heating the surface, wherein contaminants are formed on the surface;.

20. (Original) The process of claim 19 wherein the nitrogen-containing gas comprises nitrogen fluoride.

21. (Canceled)

22. (Previously presented) The process of claim 19 wherein a duration of the step (a) is between about 20 seconds and 80 seconds.

23. (Canceled)

24. (Previously presented) The process of claim 19 wherein the step (a) is practiced at about 700°C for a duration of about 20 seconds at a flow rate of about 200 sccm.

25. (Original) The process of claim 19 wherein the surface comprises a surface of a material layer selected from among a doped epitaxial material, an un-doped epitaxial material, a doped bulk silicon substrate and an un-doped bulk silicon substrate.

26. (Previously presented) The process of claim 19 wherein the polysilicon layer is selected from between a doped polysilicon material and an un-doped polysilicon material.

27. (Canceled)

28. (Previously presented) The process of claim 19 wherein the steps (a) and (b) are practiced at about an equivalent pressure.

29. (Canceled)

30. (Previously presented) The process of claim 19 wherein the polysilicon layer comprises an arsenic-doped polysilicon material.

31. (Previously presented) The process of claim 19 wherein the step (a) further comprises

(a1) exposing the surface to a nitrogen-containing gas at a flow rate of about 200 sccm to remove contaminants from the surface; and

(a2) subjecting the surface to a hydrogen bake.

32. (Previously presented) The process of claim 31 wherein the hydrogen bake comprises supplying hydrogen for a duration of about 60 to 90 seconds at a temperature of about 700°C.

33. (Previously presented) The process of claim 31 wherein the polysilicon layer is selected from between a doped polysilicon material and an un-doped polysilicon material.

34. (Previously presented) The process of claim 31 wherein the steps (a1) and (a2) are performed in-situ.

35 (New) A process for removing contaminants from a surface of a first material layer having a SiGe layer during fabrication of an integrated circuit prior to depositing a second material layer having an As-doped polysilicon layer thereover, the process comprising steps of:

(a) cleaning the surface;

(b) forming a hydrogen termination on the surface;

(b2) pre-heating the surface, wherein contaminants are formed on the surface;

(c) exposing the surface to a nitrogen-containing gas at a temperature of between about 500°C and 800°C to remove the contaminants from the surface;

(d) depositing the second material layer within the temperature range of the step (c); and

(e) wherein the steps (c) and (d) are performed in a single deposition chamber.